What is claimed is:

1. A method of detecting an error in a data stream, the method comprising:

parsing input data packets while looking for a data packet having a predetermined format; and

enabling an error-checking hardware module upon detecting an input data packet having the predetermined format.

2. The method of Claim 1, wherein the error-checking hardware module inserts an error status flag into a data packet if an error is detected.

3. The method of Claim 2 further comprising decoding the data packets according to the inserted error status flags.

4. The method of Claim 1 further comprising selecting audio data from the input data packets and storing the audio data in a designated storage location.

5. The method of Claim 1, wherein the predetermined format is AC-3 format and the error-checking hardware module is configured to perform cyclic redundancy check.

6. The method of Claim 1, wherein the error-checking hardware module is configured to perform cyclic redundancy check at bit level.

7. The method of Claim 6, wherein the cyclic redundancy check comprises:

creating at least a one-cycle delay; and

subjecting each bit of the data packets to polynomial division.

8. The method of Claim 1, wherein the input data packets comprise one or more of a sub-picture frame, a user data frame, a video frame, and an audio frame.

9. The method of Claim 1 further comprising decrypting and demultiplexing the input data packets.

10. A method of checking errors in a data stream, the method comprising:

checking data frames for errors;

inserting an error flag into each data frame to create a flagged data frame upon detecting an error;

storing each flagged data frame in a memory unit; and

decoding each flagged data frame by reading the data from the memory unit and processing the flagged data frame based on the error flag.

11. The method of Claim 10 further comprising checking for data frames having AC-3 format before checking for errors.

12. The method of Claim 10 further comprising detecting an error in the data frame using polynomial division.

13. The method of Claim 10 further comprising performing cyclic redundancy check on each bit of data.

14. A method of decoding a data stream, the method comprising:

flagging errors in a data stream to generate a flagged data frame; and

decoding a data frame by processing the flagged data frame differently from data frames that do not contain an error.

15. An apparatus for detecting an error in a data stream, the apparatus comprising:

a parser unit for parsing the data stream to identify a data frame having a predetermined format;

an error-checking module that becomes enabled if the parser unit identifies a data frame having the predetermined format, wherein the error-checking module inserts an error status flag in the data frame upon finding an error; and

a decoder for decoding the data stream according to the error status flag.

16. The apparatus of Claim 15 further comprising:

an interface module that demultiplexes the data frames; and

a memory control module that is coupled to the interface module and the decoder to store raw and decoded data.

17. The apparatus of Claim 16 further comprising a first bus and a second bus connected to the decoder, wherein the first bus is a control bus for transmitting control and parameter data to a control register and the second bus is configured to transmit data between the memory control module, the interface module, and the parser unit.

18. The apparatus of Claim 16 further comprising a first processor and a second processor, wherein the first processor is programmed to decode audio data and the second processor is programmed to decode video data.

19. The apparatus of Claim 18 further comprising hardware modules configured to perform video decoding, the hardware modules communicating with the second processor to decode video data while the decoder is decoding audio data.

20. The apparatus of Claim 16 further comprising a memory unit that stores data frames with error status flags and makes the data frames accessible to the error-checking module.

21. The apparatus of Claim 15, wherein the parser unit and the error-checking module are connected in parallel and receive the same data.

22. The apparatus of Claim 15, wherein the predetermined format is AC-3 audio format.

23. The apparatus of Claim 15, wherein the error-checking module comprises:

an array of flip-flops to retain bits of data and create a delay;

a selector coupled to the array for sequentially selecting one bit;

a counter coupled to the selector to determine the number of bits operated on; and

a gate array configured to perform polynomial division on each sequential bit of data.